

Abstracts

High-Speed Enhancement-Mode GaAs MESFET Logic

T. Mizutani, N. Kato, M. Ida and M. Ohmori. "High-Speed Enhancement-Mode GaAs MESFET Logic." 1980 Transactions on Microwave Theory and Techniques 28.5 (May 1980 [T-MTT] (Special Issue on Gigabit Logic for Microwave Systems)): 479-483.

High-speed enhancement-mode GaAs MESFET logic circuits have been fabricated by electron beam lithography. A 15-stage ring oscillator composed of 0.8- μ m gate length and 40- μ m gate width inverters has given a minimum propagation delay time of 77 ps at a power dissipation of 977 μ W. A minimum power-delay product of 1.6 fJ has been obtained with a 20- μ m gate width circuit at a propagation delay time of 200 ps. Liquid nitrogen temperature operation has also been performed, and a speed almost twice higher than that at room temperature has been obtained. The minimum propagation delay time was 51 ps, and the associated power dissipation was 1.9 mW.

[Return to main document.](#)